the masks 26, 28 covering the conductive pads 16, 22, respectively, have a major axis 32 and a minor axis 34. The major axis 32 has a first dimension 36 that is greater than the diameter 38 of the conductive pads 16, 22. The regions of the conductive pads 16, 22 proximate the major axis 32 of the conductive pads 16, 22 are exposed or "un-captured" by the masks 26, 28. In contrast, the minor axis 34 has a second dimension 40 that is less than the diameter 42 of the conductive pads 16, 22. In regions 44, the conductive pads 16, 22 are partially covered or "captured" by the masks 26, 28.--

IN THE CLAIMS:

Please cancel claims 23 and 26.

Please amend the claims as follows:

14. (Twice Amended) An integrated chip package comprising:

a first substrate and a second substrate;

a mask on a surface of at least one of the first and second substrates, wherein the mask includes a plurality of elongated openings; and

a plurality of interconnections between the first and second substrates.

15. (Amended) The integrated circuit chip package of claim 14, wherein the plurality of partially captured pads are formed by a mask having non-circular mask openings.